

**MODELING CACHE COHERENCE
PROTOCOL
USING PREDICATE/TRANSITION NETS**

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0. ARCHITECTURES OF MULTIPROCESSORS WITH PRIVATE CACHES AND INTERCONNECTION NETWORKS

1. TOP-DOWN DESCRIPTION AND MODELING OF THE PROTOCOL USING Pr/T NETS.

2. DESCRIPTION OF COMPLEX SYNCHRONIZATION OF THE ARCHIBALD'S PROTOCOL.

3. DERIVATION OF INVARIANTS DIRECTLY FROM THE Pr/T NET WITHOUT UNFOLDING IT.

4. BEHAVIORAL PROPERTIES OF CACHE COHERENCE PROTOCOL ARE STUDIED (CORRECTNESS, FAIRNESS, BOUNDS FOR THE HARDWARE RESOURCES).

CACHE REPLACEMENT POLICIES

1. WRITE THROUGH (WT) – Main Memory is updated each time a processor performs a write access; up-to-date information can be obtained:

- from Main Memory**
- listening to bus exchanges (snooping caches).**

2. WRITE BACK (WB) - a complete block update is only required when a modified block must be replaced or accessed by another cache.