CIS 525 Parallel and Distributed Software Development

MODELING CACHE COHERENCE PROTOCOL USING PREDICATE/TRANSITION NETS

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CACHE REPLACEMENT POLICIES

1. WRITE THROUGH (WT) – Main Memory is updated each time a processor performs a write access; up-to-date information can be obtained:

- **from Main Memory**
- **listening to bus exchanges (snooping caches).**

2. WRITE BACK (WB) - a complete block update is only required when a modified block must be replaced or accessed by another cache.